REMARKS/ARGUMENTS

Claims 1-6, 8, 10-15 and 17-22 are now pending in the present application. Claims 1, 2, 6, 8, 10, 11, 15, 17 and 18-20 were amended; and claims 7, 9 and 16 were canceled to expedite prosecution. No claims were added. Applicants have carefully considered the cited art and the Examiner's comments and believe the claims patentably distinguish over the references and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

Amendments were made to pages 1 and 2 of the specification to complete the identification of related applications referred to therein. No new matter has been added by any of the amendments to the specification.

I. Double Patenting

The Examiner has provisionally rejected claims 1, 3-8, 10, 12-18 and 20-22 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5, 7, 9, 11-15 and 17-20 of copending Application Serial No. 10 /704,117 in view of Torrey et al. (U.S. Patent No. 6,145,123). This provisional rejection is respectfully traversed.

Initially, commonly assigned Patent Application S.N. 10/704,117 was, at the time the claimed invention was made, commonly owned by International Business Machines Corporation. U.S. Patent Application Serial No. 10 /704,117, accordingly, does not qualify as prior art with respect to the present application.

In addition, independent claims 1, 10 and 18 have been amended to more clearly distinguish the present invention over the cited art, and Applicants respectfully submit that claims 1, 3-6, 8, 10, 12-15, 17-18 and 20-22 do not conflict with claims of U.S. Patent Application Serial No. 10/704,117 and patentably distinguish over Claims 1-5, 7, 9, 11-15 and 17-20 of U.S. Patent Application Serial No. 10/704,117 in view of Torrey.

In rejecting claim 1, the Examiner asserts that the copending application discloses all the same limitations as the limitations of claim 1 with the exception of the limitation "said processor being in the data processing system, said indicator indicates enabling a mode of operation in which interrupts are to be generated, and responsive to receiving a subsequent instruction after receiving the instruction". The Examiner contends, however:

> Torrey discloses an information processing system with trace on/off control (see Abstract), wherein responsive to receiving an instruction for execution in an instruction cache (i.e., Core 172 of Fig. 1) in a processor (i.e., Processor 110 of Fig. 1) being in a data processing system (i.e., information processing system 600 of Fig. 6; See col. 5, lines 9-11), determining whether the instruction indicates enabling a mode of operation (i.e., turning on trace operation; See Fig. 5, Steps 530-550, and col. 10, lines 5-11) in which interrupts (i.e., debug exceptions) are to be generated (See col. 6, line 56 through col. 7, line 19); and responsive to receiving a subsequent instruction (i.e., next instruction in Step 530 of Fig. 5) after receiving the instruction (See col. 6, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said trace on/off control as disclosed by Torrey, in said data processing system, as disclosed by the instant application, for the advantage of providing a more specific and relevant trace of instruction being of the certain type (i.e., program operation) for subsequent analysis (See Torrey, col. 3, lines 45-50).

Office Action dated January 6, 2006, page 4.

Claim 1 of the present application, as amended herein, is as follows:

> 1. A method in a data processing system for processing instructions, the method comprising:
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> responsive to receiving an initial instruction for execution in an instruction cache in a processor in the data processing system, determining whether the initial instruction indicates enabling a mode of operation in which interrupts are to be generated;
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> if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated, receiving a subsequent instruction;
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> determining whether the subsequent instruction is of a type selected for analysis; and
>
> generating an interrupt if the subsequent instruction is determined to be of a type selected for analysis.

A fundamental notion of patent law is the concept that invention lies in the new combination of old elements. Therefore, a rule that every invention could be rejected as obvious by merely locating each element of the invention in the prior art and combining the references to formulate an obviousness rejection is inconsistent with the very nature of "invention." Consequently, a rule exists that a combination of references made to establish a *prima facie* case of obviousness must be supported by some teaching, suggestion, or incentive contained in the prior art which would have led one of ordinary skill in the art to make the claimed invention.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The requirements for establishing a *prima facie* case of obviousness in view of a combination of references are set forth in detail in Section 2142 of the MPEP and include the requirements that the Examiner explain in detail why the combination of the teachings is proper, that the

Examiner provide a clear and convincing line of reasoning as to why an artisan would have found the claimed invention obvious in light of the teachings of the references, and that the Examiner provide a showing that it is the prior art and not the Applicant's own disclosure that teaches the combination asserted by the Examiner.

Neither the claims of U.S. Patent Application Serial No. 10/704,117, nor Torrey nor their combination discloses or suggests, "if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated, receiving a subsequent instruction", "determining whether the subsequent instruction is of a type selected for analysis", and "generating an interrupt if the subsequent instruction is determined to be of a type selected for analysis" recited in claim 1 of the present application.

Claim 1 of U.S. Patent Application Serial No. 10/704,117 recites, in part, "generating an interrupt if the indicator is associated with the instruction and the instruction is of the certain type within the range of instructions". Claim 1 of the present application, on the other hand, recites "receiving a subsequent instruction" if an initial instruction indicates enabling a mode of operation in which interrupts are to be generated, and then "determining whether the subsequent instruction is of a type selected for analysis". An interrupt is then generated "if the subsequent instruction is determined to be of a type selected for analysis".

The claims of U.S. Patent Application Serial No. 10/704,117 are not directed to receiving a subsequent instruction and determining if the subsequent instruction is of a type selected for analysis, and then generating an interrupt if the subsequent instruction is determined to be of a type selected for analysis. Claim 1 of the present application, accordingly, recites an invention that is quite different from and that is patentably distinct from the claims of U.S. Patent Application Serial No. 10/704,117.

Furthermore Torrey does not supply the deficiencies in the claims of U.S. Patent Application Serial No. 10/704,117. Torrey does not disclose "if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated, receiving a subsequent instruction", and "determining whether the subsequent instruction is of a type selected for analysis" as now recited in claim 1. The Examiner points to Step 530 in Figure 5 of Torrey as corresponding to the subsequent instruction recited in the claim. With respect to Step 530, Torrey states in col. 10, lines 5-11:

> Prior to execution of each instruction, the address of each instruction is checked for a matching address stored in a debug register during check breakpoint operation **530**. If the address of the next instruction to be executed is determined to match the address stored in DR4, at check DR4, decision **540**, the trace function is turned on at turn on trace operation **550**.

As is apparent from the above description, Torrey does not disclose making a determination whether a subsequent instruction (that is received if an initial instruction "indicates enabling a mode of operation in which interrupts are to be generated", "is of a type selected for analysis", and does not disclose generating an interrupt "if the subsequent instruction is determined to be of a type selected for analysis". The "next" instruction in Torrey is simply a "next instruction to be executed".

Torrey, accordingly, does not supply the deficiencies in the claims of U.S. Patent Application Serial No. 10/704,117 as presently recited, and claim 1 patentably distinguishes over the claims of U.S. Patent Application Serial No. 10/704,117 in view of Torrey in its present form.

Independent claims 10 and 18 have been amended in a similar manner to claim 1, and patentably distinguish over the claims of U.S. Patent Application Serial No. 10/704,117 in view of Torrey for similar reasons as discussed above with respect to claim 1. Dependent claims 3-6, 8, 12-15, 17 and 20-22 also patentably distinguish over he claims of U.S. Patent Application Serial No. 10/704,117 in view of Torrey, at least by virtue of their dependency.

Therefore, the provisional rejection of claims 1, 3-8, 10, 12-18 and 20-22 as being unpatentable over claims of U.S. Patent Application Serial No. 10/704,117 in view of Torrey has been overcome.

II. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 3-6, 8-10, 12-15, 17-18, and 20-22 under 35 U.S.C. § 102(b) as being anticipated by Smolders (U.S. Patent No. 6,253,338 B1). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> *Referring to claim 1,* Smolders discloses a method in a data processing system for processing instructions (i.e., method within a data processing system for counting various events from a running program; See Abstract), the method comprising:
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> - responsive to receiving an instruction for execution in an instruction cache (i.e., L1 Cache 66 of Fig. 2) in a processor (i.e., Processor 12 of Fig. 2) in the data processing system (i.e., Data Processing System 10 in Fig. 1; see col. 3, lines 4-13), determining whether the instruction (i.e., instruction for setting a specified branch trace enable bit 80 in the machine state register 76 in Fig. 2) indicates enabling a mode of operation (i.e., branch tracing mode enabled by setting BE bit in MSR) in which interrupts (i.e., trace interrupts) are to be generated (See col. 3, line 58 through col. 4, line 11);
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> - responsive to receiving a subsequent instruction after receiving the instruction (i.e., said instruction for setting BE), determining whether the subsequent instruction is of a certain type (i.e., checking for branch instructions; See col. 3, line 67 through col. 4, line 6); and

- generating an interrupt (i.e., trace interrupt) if the mode of operation in which interrupts are to be enabled and the instruction is of the certain type (See col. 3, lines 58-61).

Office Action dated January 6, 2006, pages 8-9.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Smolders does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to amended claim 1, in particular, Smolders does not teach or suggest "if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated, receiving a subsequent instruction", "determining whether the subsequent instruction is of a type selected for analysis", and "generating an interrupt if the subsequent instruction is determined to be of a type selected for analysis".

Smolders is directed to a mechanism for tracing hardware counters by way of an interrupt without introducing overhead or modifying the code being counted. In rejecting claim 1, the Examiner interprets "setting BE bit" as enabling a mode of operation in which interrupts are to be generated. The Examiner then refers to "checking for trace instructions" as described in col. 3, line 67 through col. 4, line 6 of Smolders as corresponding to determining whether a subsequent instruction is of a certain type. Col. 3, line 61-col. 4, line 6 of Smolders states as follows:

> When using a processor different than the POWERPC 604, used herein by way of example only, if such processor used does not have a branch tracing mode, i.e. the equivalent of the BE bit in the MSR and an automatic trace interruption, after each branch, the processor would be programmed in single-step mode, i.e. to generate a trace interruption after each instruction. In such a case, the code handling the trace interruptions will have to check for branch instructions. When a branch is found, the flow of execution proceeds as described below in **Fig. 3**, if the instruction was not a branch, the flow of execution simply returns to the next instruction, in sequence without any additional action.

Amended claim 1 recites that a subsequent instruction is received "if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated", and further, that a

determination is made whether "the subsequent instruction is of a type selected for analysis". An interrupt is then generated "if the subsequent instruction is determined to be of a type selected for analysis". Smolders, on the other hand, as clearly indicated in the above recitation, describes an automatic trace interruption or generating a trace interruption after each instruction. Smolders does not disclose making a determination whether a subsequent instruction (that is received if an initial instruction indicates enabling a mode of operation in which interrupts are to be generated) is of a type selected for analysis, or generating an interrupt "if the subsequent instruction is determined to be of a type selected for analysis". Smolders, accordingly, does not anticipate claim 1, and claim 1 should be allowable over Smolders in its present form.

Claims 3-6 and 8 depend from and further restrict claim 1, and are also not anticipated by Smolders, at least by virtue of their dependency..

Independent claims 10 and 18 have been amended in a manner similar to claim 1, and are also not anticipated by Smolders for similar reasons as discussed above with respect to claim 1. Claims 12-15, 17 and 20-22 depend from and further restrict one of claims 10 and 18 and are also not anticipated by Smolders, at least by virtue of their dependency.

Therefore, the rejection of claims 1, 3-6, 8-10, 12-15, 17-18, and 20-22 under 35 U.S.C. § 102 has been overcome.

Furthermore, Smolders does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Smolders actually teaches away from the presently claimed invention because it teaches "an automatic trace interruption after each branch" or generating a trace interruption "after each instruction" as opposed to generating an interrupt if a subsequent instruction is determined to be of a type selected for analysis as in the presently claimed invention. Absent the Examiner pointing out some teaching or incentive to modify Smolders to determine whether a subsequent instruction is of a type selected for analysis, and to generate an interrupt if the subsequent instruction is determined to be of a type selected for analysis, one of ordinary skill in the art would not be led to modify Smolders to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify Smolders in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

III. 35 U.S.C. § 103, Obviousness – Claims 2, 11 and 19

The Examiner has rejected claims 2, 11, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Smolders (U.S. Patent No. 6,253,338 B1) as applied to claims 1, 3-6, 8-10, 12-15, 17-18, and 20-22

above, and further in view of Torrey et al. (U.S. Patent No. 6,145,123). This rejection is respectfully traversed.

Claims 2, 11 and 19 depend from and further restrict claims 1, 10 and 18, respectively. Torrey does not supply the deficiencies in Smolders as discussed above. Claims 2, 11 and 19, accordingly, are allowable over the references, at least by virtue of their dependency on allowable claims.

Therefore, the rejection of claims 2, 11, and 19 under 35 U.S.C. § 103 has been overcome.

IV. 35 U.S.C. § 103, Obviousness – Claims 7 and 16

The Examiner has rejected claims 7 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Smolders (U.S. Patent No. 6,253,338 B1) as applied to claims 1, 3-6, 8-10, 12-15, 17-18, and 20-22 above, and further in view of Adl-Tabatabai et al. (U.S. Patent No. 6,928, 582 B2). This rejection is respectfully traversed.

Claims 7 and 16 have been canceled to expedite prosecution. Therefore, the rejection of claims 7 and 16 under 35 U.S.C. § 103 has been overcome.

V. Conclusion

For all the above reasons, it is respectfully urged that claims 1-6, 8, 10-15 and 17-22 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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